globetech SOLUTIONS

Verification Intellectual Property Products

UART 16x50 *e*VC

e Verification Components

Globetech Solutions' *e*VCs are independent, pre-verified, re-usable, verification environments that can be readily integrated into your design.

Maintaining full compatibility with Cadence's Incisive Specman Simulator™, these components provide a solid basis for forming and realizing a complete, reliable and re-usable verification strategy.

e Reuse Methodology

Globetech Solutions' *e*VCs comply with Cadence's *e* Reuse Methodology (*e*RM™). The *e*RM ensures that *e*VCs seamlessly plug-and-play and operate consistently with all *e*RM compliant verification environments by applying consistent terminology, architecture, coding style and packaging.

cadence OPENCHOICE

Why *e*VCs?

There are many advantages to choosing a Globetech Solutions *e* Verification Component:

Time to silicon - dramatically reduce the verification cycle

Flexibility - quickly create and fine tune a variety of test scenarios

Risk Management - pre-verified components help reduce problem space

Re-usability - spend your time creating new tests, not environments!

Full Support - integration, training and support to ensure your success

The UART *e*VC

The Universal Asynchronous Receiver Transmitter (UART) 16x50 *e*VC is a complete device-level verification environment capable of validating industry standard 16550 through 16950 A-D UART designs. The UART 16x50 *e*VC is a ready-to-use, proven, IP core verification environment that can boost productivity by including advanced features such as fully prioritized interrupt handling and direct memory access support.

Features

- ✓ Compatible with industry standard UART 16550 through 16950 A-D devices
- ✓ Written in *e* and fully compatible with Cadence Incisive Specman Simulator - HDL independent
- ✓ Device-level: Can be used to verify complete UART IP cores comprising a serial and a processor interface
- ✓ Serial interface agent provides constrained-random UART frame sequence generation with error injection and auto-flow support
- ✓ Processor Driver Abstraction Layer (DAL) architecture provides high-level generation tools for test writing and monitoring at the processor bus interface
- ✓ Independent monitor with built-in device reference model for enhanced checking and functional coverage collection
- ✓ Support for up to 128-byte transmission and reception FIFOs
- ✓ Fault start bit and break indication detection
- ✓ Independently controlled and fully prioritized interrupt handling and DMA support
- ✓ Built-in metric analysis for Coverage-Driven Verification (CDV)
- ✓ Complete and configurable error reporting, adjustable levels of tracing and verbosity

UART 16x50 *e*VC Structure

The UART 16x50 *e*VC's dual agent architecture provides constrained random sequence generation at both the serial and processor-bus interfaces. The independent monitor is capable of analyzing traffic at the device-level and includes a complete register-level reference model. Temporal and data checkers are used to perform multi-channel verification with dual interface cross-checking and collect device-level functional coverage metrics.

Verification Using the UART 16x50 *e*VC

In **Figure 1**, the UART 16x50 *e*VC is used to verify a complete UART 16550A IP core. The *e*VC's agents are used to drive both core interfaces, creating constrained-random, bidirectional, traffic flow. The two *monitors* examine traffic, scoreboard data and utilize their *checkers* to ensure adherence to the UART transmission protocol and 16550A device architecture. The monitor *coverage* modules on-the-fly track the functional aspects of the protocol that have been exercised. The *e*VC internally references the 16550A architecture to ensure full coverage of all functional aspects of the device, such as FIFO-full conditions or interrupt generation.

Benefits of the UART 16x50 *e*VC

- ✓ **Complete solution:** Capable of fully verifying UART 16550 through 16950 design cores while minimizing development time
- ✓ **Solid technology:** Built on best-of-breed technology and methodologies by Cadence Design Systems
- ✓ **Proven quality:** In strict compliance with industry quality standards and Cadence OpenChoice qualified (visit http://www.cadence.com/partners/ip_program)
- ✓ **High maturity:** Used in many silicon-proven projects

Further Information

For further information or to request an evaluation, please visit us online at www.globetechsolutions.com or call us at ++1 650 988 6900 (US) or ++30 23 10 31 35 53 (EU).

Component	Function
Serial Agent	Emulates the functionality of a device attached to the UART DUT by injecting data and control stimuli.
Monitor	Provides error checking, data score-boarding and coverage information with complete reference model.
Core	A complete UART 16x50 core in *e*. It can be used in place of DUT for training and familiarization, as well as advanced verification scenarios.
Processor Driver	This component emulates the processor behavior at the device level. It provides stimuli to the DUT, in the form of register reads and writes, creating a continuous data and control exchange path.

Note that the monitor element is required for all testing scenarios; all other elements are entirely independent and can be deployed separately.

Table 1: Functional Description of UART *e*VC Components

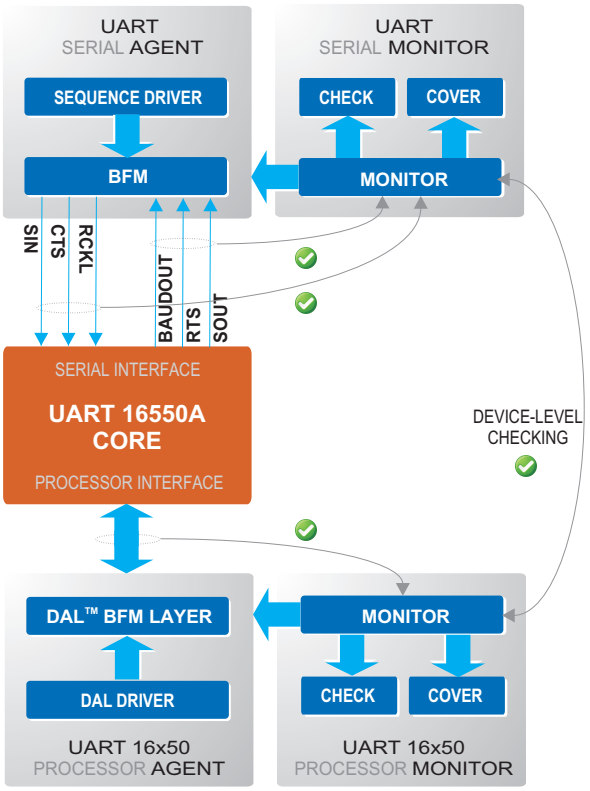

Figure 1: Verifying a 16550A IP core using the UART 16x50 *e*VC
The Serial Agent is used to drive frames to the DUT's serial interface. Conversely, the Processor Agent configures the device and initiates UART frame transmissions. The Monitor performs bidirectional communication and device-level checking.

globetech
SOLUTIONS

Corporate Headquarters
2 Kallirois St
Elaiones - Pylaia
Thessaloniki 55535
Greece
Tel: +30 23 10 31 35 53
Fax: +30 23 10 31 39 64
info@globetechsolutions.com
www.globetechsolutions.com

cadence
OPENCHOICE

Maturity	First Release	*e*RM Compliant	VPA Enabled	SB Optimized
Excellent	Aug 2002			