globetech SOLUTIONS

Verification Intellectual Property Products

IEEE 1149.7 (cJTAG) *e*VC

e Verification Components

Globetech Solutions' *e*VCs are independent, pre-verified, re-usable, verification environments that can be readily integrated into your design.

Maintaining full compatibility with Cadence's Incisive Specman Simulator™, these components provide a solid basis for forming and realizing a complete, reliable and re-usable verification strategy.

e Reuse Methodology

Globetech Solutions' *e*VCs comply with Cadence's *e* Reuse Methodology (*e*RM™). The *e*RM ensures that *e*VCs seamlessly plug-and-play and operate consistently with all *e*RM compliant verification environments by applying consistent terminology, architecture, coding style and packaging.

Why *e*VCs?

There are many advantages to choosing a Globetech Solutions *e* Verification Component:

- **Time to silicon -** dramatically reduce the verification cycle
- **Flexibility -** quickly create and fine tune a variety of test scenarios
- **Risk Management -** pre-verified components help reduce problem space
- **Re-usability -** spend your time creating new tests, not environments!
- **Full Support -** integration, training and support to ensure your success

The IEEE 1149.1 (JTAG) *e*VC

Originally proposed by the Mobile Industry Processor Interface (MIPI) Alliance, IEEE 1149.7™ (compact JTAG/cJTAG) extends IEEE 1149.1™ to support the needs of debug applications for products with complex digital circuitry, embedded software, and one or more CPUs. The standard addresses key challenges such as enhanced functionality for test access, reduced pin-count and improved power management.

The cJTAG *e*VC verifies logic design blocks conforming to any of the six compliance levels defined by the IEEE standard, significantly reducing time to functional closure and increasing quality of first silicon.

Features

- ☑ Written in the IEEE 1647™-2008 e language and fully compatible with Cadence Incisive Enterprise and Plan-to-Closure Methodology (IPCM)
- ☑ Fully compliant with IEEE 1149.7™-2007
- ☑ Incremental 1149.7 compliance class verification capabilities - can be used to certify any class of component
- ☑ Extended Protocol Unit (EPU) support for cJTAG classes1–3
- ☑ Supports all mandatory and optional EPU commands
- ☑ Advanced Protocol Unit (APU) support for cJTAG classes 4-5
- ☑ Supports both 4-pin and 2-pin P1149.7 interfaces
- ☑ Supports all mandatory and optional scan formats (Jscan, MScan, OScan and SScan)
- ☑ Extensive sequence library for easy test creation of both constrained-random as well as fully directed tests
- ☑ Compliance Management Suite, compatible with Cadence Incisive Enterprise Manager™
- ☑ Chip-level validation and TAP virtualization capabilities

Verification Using the cJTAG *e*VC

From developing a cJTAG TAP controller to designing a complete chip-level integrated architecture, the cJTAG *e*VC can be a valuable tool for isolating design bugs, identifying protocol compatibility issues and ensuring smooth interoperability with other system components. **Figure 1** illustrates how the cJTAG eVC can be used to verify a typical IEEE 1149.7 deployment.

Integrating the cJTAG *e*VC

The cJTAG eVC connects to three IEEE 1149.7 TAP.7 standard interfaces:

- ☑ The 1149.7 interface to off-chip DTS
- ☑ The 1149.1 interface to on-chip test logic (STL)
- ☑ The 1149.7 power control interface

In addition, the cJTAG *e*VC exports a white-box 1149.7 signaling interface for enhanced checking and debug functionality. Finally, the *e*VC provides a handy STL emulation feature, which allows users to test 1149.7 IP with a variety of STL configurations.

Compliance Management System

The Compliance Management System (CMS) quantifies compliance of IP cores to the IEEE 1149.7 specification, enabling unprecedented levels of confidence and risk management. CMS includes the following components:

- ☑ A complete compliance verification plan document, which maps coverage metrics to IEEE 1149.7 standard rules
- ☑ A compliance test-suite, which can be used to reach at least 70% compliance coverage out of the box

Component	Function
DTS Agent	Implements a self-contained Debug and Test System constrained-random pattern generator. The Agent includes the Sequence Driver and BFM modules.
DTS Sequence Driver	Generates complete control and data transactions at different levels of abstraction. For example, a `SGC SCAN_CTL STMC CMD cjtag_seq` sequence can be used to deliver a complete scan control store command to the EPU.
DTS Bus Functional Model (BFM)	Translates sequences into signal transactions with the TAP.7. Can operate in either EPU or APU mode.
cJTAG Monitor	Monitors activity at the cJTAG TAP.7 interfaces. The monitor checks strict behavior of the TAP.7 controller against normative language of the IEEE 1149.7 standard. It also generates functional and compliance coverage metrics.
cJTAG Power Manager	Manages the power control features that are defined in the IEEE 1149.7 specification (optional).

The cJTAG Monitor can be used as an observer in any existing or legacy test-bench. The DTS Agent can also be deployed separately.

Table 1: Functional Description of IEEE 1149.7 (JTAG) *e*VC Components

At any point during the verification process, users can get an accurate report of 1149.7 clauses satisfied and, perhaps more importantly, how much verification still needs to be performed before functional closure.

Further Information

For further information or to request an evaluation, please visit us online at www.globetechsolutions.com or call us at +30 23 10 31 35 53.

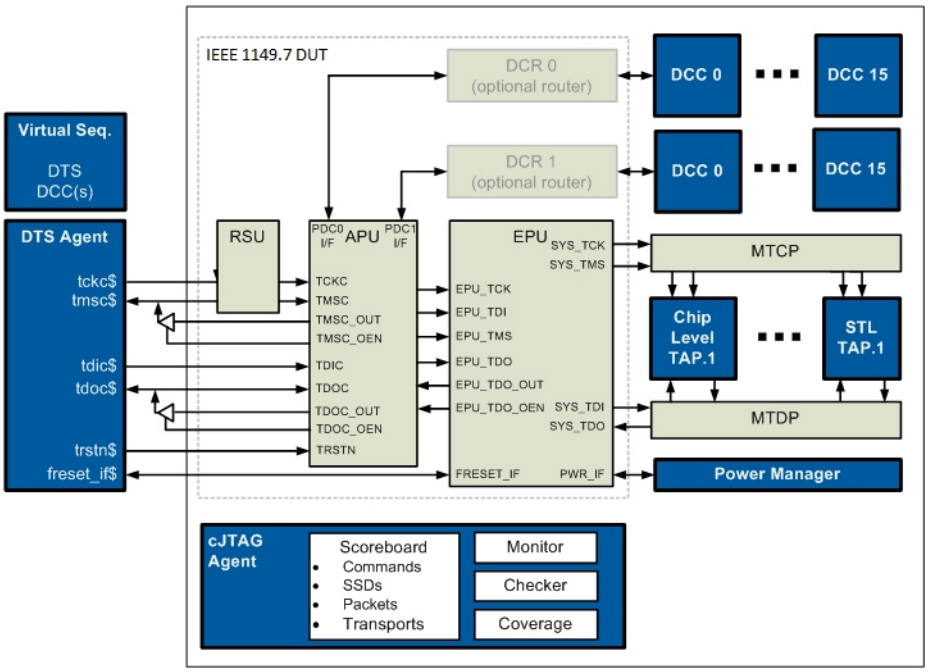

Figure 1: cJTAG *e*VC Typical Deployment

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