globetech SOLUTIONS

Verification Intellectual Property Products

CE-ATA *e*VC

e Verification Components

Globetech Solutions' *e*VCs are independent, pre-verified, re-usable, verification environments that can be readily integrated into your design.

Maintaining full compatibility with Cadence's Incisive Specman Simulator™, these components provide a solid basis for forming and realizing a complete, reliable and re-usable verification strategy.

e Reuse Methodology

Globetech Solutions' *e*VCs comply with Cadence's *e* Reuse Methodology (*e*RM™). The *e*RM ensures that *e*VCs seamlessly plug-and-play and operate consistently with all *e*RM compliant verification environments by applying consistent terminology, architecture, coding style and packaging.

cadence™ OPENCHOICE

Why *e*VCs?

There are many advantages to choosing a Globetech Solutions *e* Verification Component:

Time to silicon - dramatically reduce the verification cycle

Flexibility - quickly create and fine tune a variety of test scenarios

Risk Management - pre-verified components help reduce problem space

Re-usability - spend your time creating new tests, not environments!

Full Support - integration, training and support to ensure your success

The CE-ATA *e*VC

The Consumer Electronics Advanced Technology Attachment (CE-ATA) *e*VC is a complete verification environment capable of verifying CE-ATA compliant Host or Device implementations.

Based on a flexible architecture and taking full advantage of Cadence's Incisive Enterprise platform, the CE-ATA *e*VC is a powerful tool for design and verification engineers looking to build or integrate CE-ATA compliant silicon IP.

Features

- ✓ Written in *e* and fully compatible with Cadence Incisive Specman Simulator - HDL independent
- ✓ *e*RM compliant - Plug-n-Play
- ✓ Includes executable verification plan for Incisive Verification Manager™
- ✓ Optimized for Incisive Scenario Builder™
- ✓ Functional coverage analysis for Coverage-Driven Verification (CDV)
- ✓ Fully compliant with CE-ATA Digital Specification revision 1.1 and later
- ✓ Dual Agent architecture can be used to verify both CE-ATA compliant Hosts (Masters) and Devices (Slaves)
- ✓ CE-ATA Host Agent Sequence Driver supports constrained-random generation at both CE-ATA and MultiMedia Card (MMC) layers with error injection
- ✓ CE-ATA Device Agent emulates device behavior with integrated memory model and response generator
- ✓ Independent Monitor can be used to examine CE-ATA bus traffic in any simulation environment
- ✓ Layered Bus Protocol Checker
- ✓ Data Integrity Checker with built-in reference model of a CE-ATA Device

The CE-ATA *e*VC Structure

The CE-ATA *e*VC comprises several components in compliance with *e* Reuse Methodology (*e*RM) for maximum interoperability and reuse (see **Table 1**).

Verification Using the CE-ATA *e*VC

Implementing verification scenarios using the CE-ATA *e*VC is made easy using the features already available in the environment. Verification and design engineers can use their time more effectively writing new tests instead of building new testbenches.

In **Figure 1**, the CE-ATA *e*VC is used to verify a CE-ATA compliant Device. Hence, the *e*VC's Host Agent is configured as *Active* and is used to initiate constrained-random traffic. High-level test scenarios are translated into CE-ATA sequences and injected into the DUT by means of the BFM. The Monitor's *Checker Engine* performs layered checking for ATA rules, MMC rules, MMC timing and overall data integrity. Finally, the *Functional Coverage* engine evaluates the levels of functionality exercised during testing.

The CE-ATA *e*VC can be instantiated in several different configurations. Use the *Device* Agent to verify a CE-ATA Host design (see **Figure 2**) or a monitor-only configuration to ensure correct operation of a complete-HDL environment.

Component	Function
Agents Host or Device	Agents provide the functionality to fully emulate CE-ATA compliant Hosts or Devices. They include Sequence Drivers and BFMs, which can be fully constrained to produce any legal behavior.
Sequence Driver	In the HOST Agent, the Sequence Driver is responsible for generating CE-ATA and MMC constrained-random traffic, with error injection.
Bus Functional Model (BFM)	In either Agent, the BFM is responsible for delivering sequences on the signal interface based on the CE-ATA specification.
Monitor	The Monitor samples the communication between Host and Device entities and generates events for modules that subscribe to it, such as the *Checker*, *Functional Coverage Collector* and *Agent BFMs*.
Note that the monitor element is recommended for all testing scenarios; all other elements are entirely independent and can be deployed separately.	

Table 1: Functional Description of CE-ATA *e*VC Components

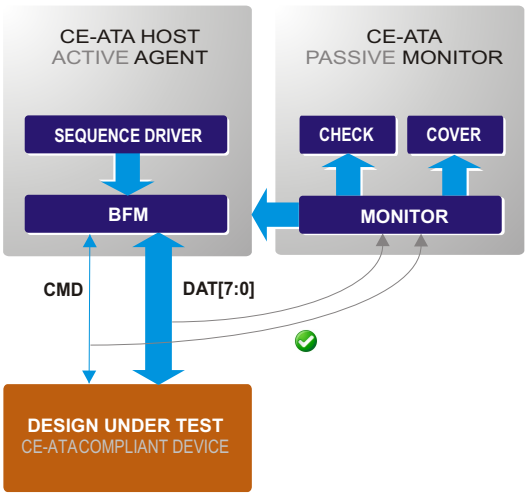

Figure 1: CE-ATA *e*VC in Host Mode Operation
The Host Agent is used to drive a CE-ATA compliant Device. The Monitor maintains a full reference model of the Device for layered protocol and device-level data checking.

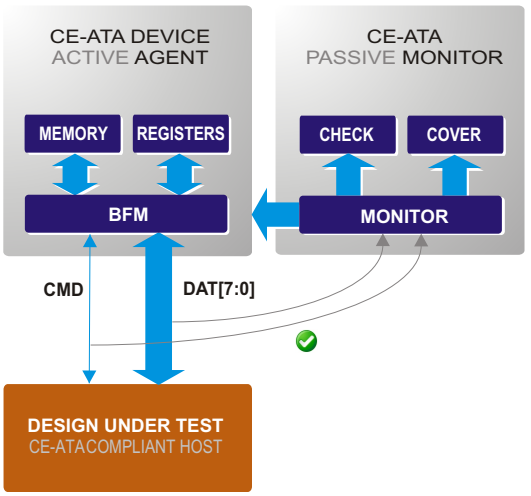

Figure 2: CE-ATA *e*VC in Device Mode Operation
The Device Agent is used to verify a CE-ATA compliant Host. The Monitor provides layered protocol checking ensuring correct operation of the Host.

Further Information

For further information or to request an evaluation, please visit us online at www.globetechsolutions.com or call us at +1 650 988 6900 (US) or +30 23 10 31 35 53 (EU).

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cadence™
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Maturity	First Release	*e*RM Compliant	VPA Enabled	SB Optimized
Good	Nov 2005	✓	✓	✓